ANALOG DEVICES

USER'S MANUAL

RTI-1260

RTI-1262

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USER'S MANUAL
RTI-1260

RTI-1262

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UNPACKING PROCEDURES

CAUTION – Some of the components assembled on RTI-1260 series cards are sensitive to electrostatic discharge and damage may occur on unconected boards subject to a high energy electrostatic field. Unused cards should be stored in the same conductive plastic bag as shipped.

When the board is to be laid on a bench for configuring, etc., it is suggested that the plastic shipping bag be inserted under the card to provide a conductive shunt.

CHAPTER 1

INTRODUCTION – SCOPE OF THE MANUAL

The RTI-1260/1262 are Analog I/O Cards compatible to the STD bus.

The intent of this manual is to serve as a guide to the proper configuration and operation as well as presenting the functional theory, specifications and application examples. Appendixes are provided which contain schematics, a multiplexer configuration tutorial and a digital code table.

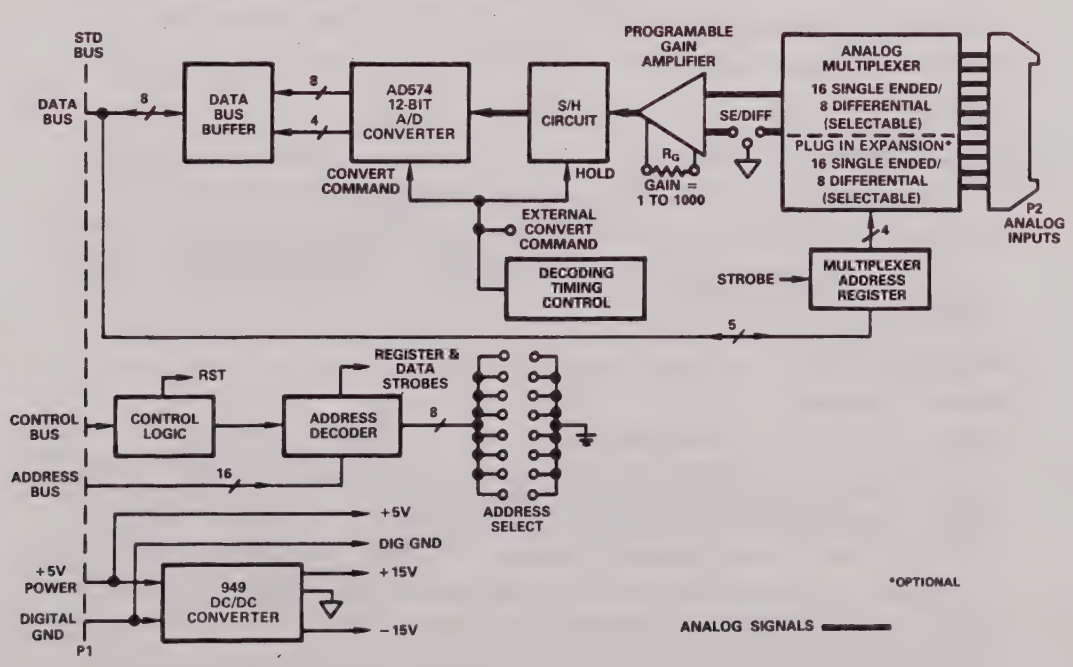
1.1 GENERAL DESCRIPTION OF THE RTI-1260/1262

The RTI-1260 Analog Input Card provide data acquisition of analog signals from up to 32 single-ended or 16 differential voltage inputs. User configurable gains of 1 to 1000 allow input ranges from 10 millivolts to 10 volts. A sample and hold amplifier and 12-bit A/D converter provide throughputs up to 25,000 channels per second.

The RTI-1262 Analog Output Card contains four 12-bit D/A converters which provide four independent output channels of analog voltage. In addition, two channels can be configured for 4-20mA outputs.

The RTI-1260 and RTI-1262 Analog Cards come complete with their own dc/dc converter, allowing the boards to operate directly from the microcomputer +5 volt supply. The cards interface to the STD bus as either a memory mapped or I/O port peripheral through a user-selection jumper option.

1.2 RTI-1260 FUNCTIONAL DESCRIPTION



RTI-1260 Block Diagram

1.2.1 MULTIPLEXER

There are three ways to configure the input multiplexer: signle-ended, differential and pseudo-differential. In the *single-ended mode*, sixteen separate analog signals may be randomly selected with reference to a common ground. For noiser environments, the *differential mode* can be used to reduce the effects of noise and bias current. This mode reduces the channel capacity to 8 inputs. The *pseudo-differential* mode takes advantage of differential inputs and provides a full 16 channel input capacity. It is necessary that all input signals have a common reference point.

This dielectrically isolated multiplexer can handle up to ±35V signals without damage (±20V with power off).

CHANNEL EXPANSION

The channel capacity on the RTI-1260 can be *doubled* by ordering the MULTIPLEXER EXPANSION KIT (ADI P/N OA10). This kit contains two multiplexer ICs which plug into on-board sockets.

1.2.2 PROGRAMMABLE GAIN AMPLIFIER (PGA)

User configured gains of 1 to 1000 are accomplished by inserting a single gain resistor on the board. This results in an effective full scale input range for ±10mV to ±10V.

1.2.3 SAMPLE-HOLD CIRCUIT (S/H)

The Sample and Hold Circuit "freezes" the analog input signal so that it can be convered by the A/D without error. The RTI-1260 has a built in circuitry to delay the convert command until the input section has settled and the S/H has acquired the signal.

1.2.4 ANALOG/DIGITAL CONVERTER (A/D)

The RTI-1260 contains a fast, 12-bit, successive approximation, analog to digital convert. The A/D resolution of 1 part in 4096 used with the PGA provides a least significant bit weighing of 4.88μV at the ±10V range. The user can select one of two A/D input ranges and one of three digital output codes with wire-wrap jumpers.

1.2.5 POWER SUPPLY (DC/DC)

The microcomputers +5V supply is all that is required to power the RTI-1260 series cards. An on-board dc/dc converter is supplied with each card to convert the +5 volt bus supply to a low noise, isolated ±15 volts required by the analog circuitry.

1.2.6 BUS INTERFACE

Mode of Operation

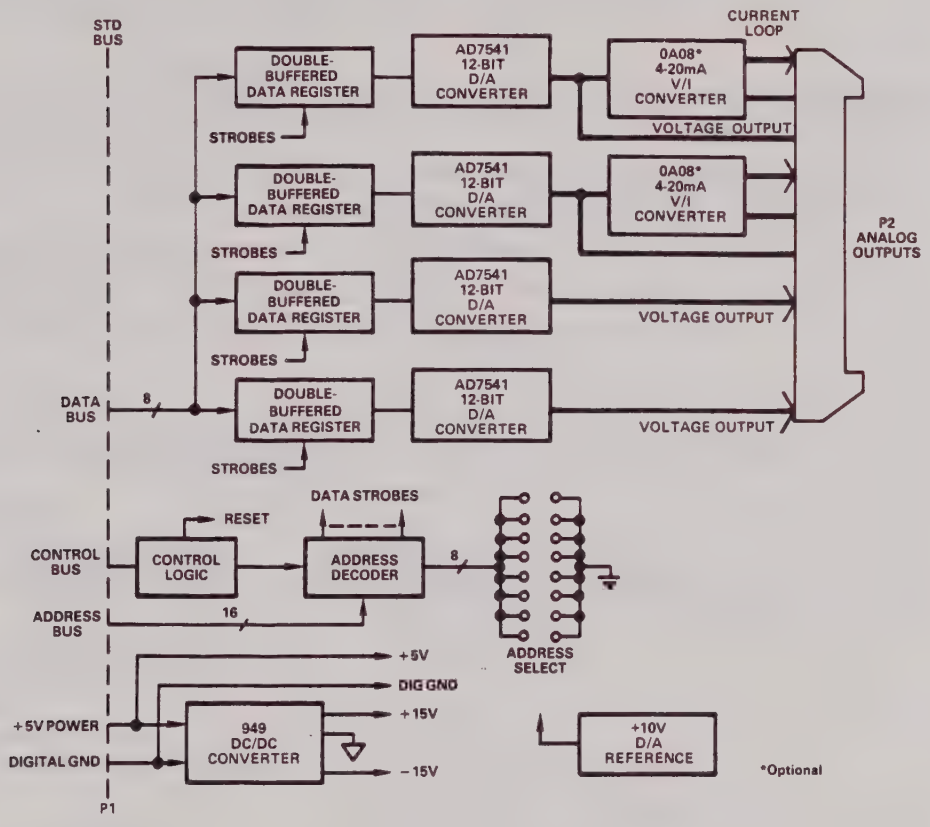
The RTI-1260 uses a memory mapped or port I/O interface scheme to communicate with the STD microcomputer. In the memory map mode, the RTI card is treated as a block of memory, simple memory read or write instructions (STA, LDA) can be used. Memory mapping also allows programmers to access the RTI boards using any of the memory reference instructions in the repertoire (SHLD, LHLD, MOV M, r, MOV r, M).

The RTI-1260 cards occupy 16 consecutive bytes of memory. Their address is determined by on-board jumpers which can be configured for an address in any

one of 256 locations in 64K of memory space.

In the port-mapped I/O mode, the RTI card is treated as 16 consecutive I/O ports, whose address is determined by jumpers. The RTI card can decode either an 8- or 16-bit I/O address.

1.3 RTI-1262 FUNCTIONAL DESCRIPTION



RTI-1262 Block Diagram

1.3.1 D/A REGISTERS

The D/A converters inputs are software driven via double buffered registers. The buffers allow two data bytes to be loaded simultaneously into the D/A converter so that the output changes directly from one 12-bit value to another.

1.3.2 DIGITAL/ANALOG CONVERTER (D/A)

The RTI-1262 contains four CMOS 12-bit D/A converters. Each D/A output can be independently selected. The user has four output voltage ranges from which to select. The 12 bits of resolution provide least significant bit values down to 1.22mV.

1.3.3 CURRENT OUTPUT (V/I)

It is often desirable to transmit an analog signal as a current rather than a voltage since noise and IR drops in the cable and connectors will not degrade the accuracy of a current signal.

Two of the four voltage outputs can be converted to a 4-20mA current loop output. These voltage to current modules (ADI P/N OA08) meet all requirements of the ISA-S50. 1 Standard for Type 3, Class L, nonisolated 4-20mA current loop

transmitters which makes them ideal for use in process and control applications. A user supplied 16 to 30 volt supply is required to power this loop.

1.3.4 POWER SUPPLY (DC/DC)

The microcomputers +5V supply is all that is required to power the RTI-1260 series cards. An on-board dc/dc converter is supplied with each card to convert the +5 volt bus supply to a low noise, isolated ±15 volts required by the analog circuitry.

1.3.5 BUS INTERFACE

Mode of Operation

The RTI-1262 uses a memory map or port I/O interface scheme to communicate with the STD microcomputer. In the memory map mode, the RTI card is treated as a block of memory, simple memory read or write instructions (STA, LDA) can be used. Memory mapping allows programmers to access the RTI cards using any of the memory reference instructions in the repertoire (SHLD, LHLD, MOV M, r, MOV r, M).

The RTI-1262 cards occupy 16 consecutive bytes of memory. Their address is determined by on-board jumpers which can be configured for an address in any one of 256 locations in 64K of memory space.

In the port-mapped I/O mode, the RTI card is treated as 16 consecutive I/O ports, whose address is determined by jumpers. The RTI card can decode either an 8- or 16-bit I/O address.

CHAPTER 2

SPECIFICATIONS

2.1 RTI-1260 SPECIFICATIONS

SPECIFICATIONS (typical @ 25°C with nominal supply voltage unless otherwise noted)

RTI-1260 ANALOG INPUT CARD	
Number of Input Channels	16 Single-Ended or 8 Differential (Jumper Selectable) Expandable to 32 Single-Ended or 16 Differential Using Two Plug-In Multiplexers (ADI Part #OA10)
Input Overvoltage Protection[1]	± 35V (Dielectrically Isolated)
Input Impedance	$>10^8\Omega$
Input Bias Current	± 50nA
Analog Connector	3M #3433, 50 pin
A/D Input Ranges[2]	0 to + 10V, ± 10V
A/D Resolution	12 Bits (4096 Counts)
A/D Output Codes[2]	Binary, Offset Binary, Two's Complement
Instrumentation Amplifier Gain Ranges	1 to 1000V/V (Resistor Programmable Gain)
Gain Equation	$G = 1 + \frac{20k\Omega}{R_G}$
A/D Conversion Time	25µs
System Throughput[3]	25,000 Channels/sec (G < 150) 20,000 Channels/sec (150 < G > 300) 11,000 Channels/sec (G = 1000)
Common Mode Voltage (CMV)	± 10V min
Common Mode Rejection (CMR)	78dB
Linearity	± 1/2LSB
Differential Nonlinearity	± 1LSB
Total System Error (Adjustable to Zero)	± 0.01% of FSR (Gain = 1 to 10) ± 0.05% of FSR (Gain = 100) ± 0.1% of FSR (Gain = 1000)
Temperature Coefficient	
Gain	± 30ppm/°C of FSR (G = 1)
Offset	± 100ppm/°C of FSR (G = 1000) ± 10ppm/°C of FSR (G = 1) ± 100ppm/°C of FSR (G = 1000)
INTERFACE PARAMETERS	
Compatibility	Meets all Electrical and Mechanical STD Bus Specifications
Implementation	Memory Mapped I/O Compatible with All CPU Types Port Mapped I/O Compatible with 8080, 8085, 8086 and Z-80 Family of CPUs
Address Selection	3 Contiguous Bytes in a 16 Byte Block. (Jumper Selectable in Any One of 256 Locations in 64K of Memory Space.)
Port Selection	3 Contiguous Ports in a 16 Port Block (Jumper Selectable on Any 16 Port Boundary in Either an 8-Bit or 16-Bit Port Image.)
Expansion Options	MEMEX and IOEXP Fully Supported with Jumper Selectable Enable High, Enable Low or Ignore Expansion Options.
POWER REQUIREMENTS	+ 5V ± 5% @ 450mA (On-Board dc/dc Converter Generates an Isolated ± 15V to Power the Data Acquisition Components.)
TEMPERATURE	
Operating	0 to + 70°C
Storage	− 55°C to + 85°C
RELATIVE HUMIDITY	Meets or Exceeds MIL-STD 202 Method 103

NOTES

[1]Specified with power applied, ± 20V with power off.

[2]User selectable with wire-wrap jumpers.

[3]Does not include CPU latency time.

Specifications subject to change without notice.

SPECIFICATIONS (typical @ 25°C with nominal supply voltage unless otherwise noted)

RTI-1262 ANALOG OUTPUT CARD	
Number of Output Channels	4
D/A Resolution	12 Bits (4096 Count)
D/A Input Codes[1]	Binary, Offset Binary
Output Voltage Range[1]	0V to +5V, 0V to +10V, ±5V, ±10V @5mA
Output Current Range[2]	4-20mA Using 2 Voltage-to-Current Modules
(Optional – 2 Channels Only)	(ADI Part #OA08)
Analog Connector	3M #3429, 26 pin
Nonlinearity	±1/2LSB
Differential Nonlinearity	±1/2LSB
Output Settling Time	25μs (to ±1/2LSB)
Gain Error (Adjustable to Zero)	±0.01% of FSR (Full Scale Range)
Offset Error (Adjustable to Zero)	±0.02% of FSR
Temperature Coefficient	
Gain	±15ppm/°C of FSR
Offset	±25μV/°C
INTERFACE PARAMETERS	
Compatibility	Meets all Electrical and Mechanical STD Bus Specifications
Implementation	Memory Mapped I/O Compatible with All CPU Types
Address Selection	8 Contiguous Bytes in a 16 Byte Block. (Jumper Selectable in Any One of 256 Locations in 64K of Memory Space)
POWER REQUIREMENTS	+5V ±5% @ 550mA (On-Board dc/dc Converter Generates an Isolated ±15V to Power the Data Acquisition Components)
TEMPERATURE	
Operating	0 to +70°C
Storage	−55°C to +85°C
RELATIVE HUMIDITY	Meets or Exceeds MIL-STD 202 Method 103

NOTES
[1]User selectable with wire-wrap jumpers.
[2]Solder in option, +16V to +30V loop power required.
Specifications subject to change without notice.

CHAPTER 3

FACTORY CONFIGURATIONS

3.1 RTI-1260

Since the RTI-1260 has been designed to be configured for different modes of operation, the board will be shipped with wire jumpers preconfigured at the factory for specific modes as follows:

Input Multiplexer Configuration	16 S.E.
PGA Gain	1V/V
Convert Command Delay	15μs
A/D Input Code	±10V
A/D Output Code	Offset Binary
Base Address	FFFO
Interface	Memory-Mapped

3.2 RTI-1262

Since the RTI-1262 has been designed to be configured in different modes of operation, the board will be shipped with wire jumpers preconfigured at the factory for specific modes as follows:

D/A Output Range	±10V
D/A Input Code	Offset Binary
Base Address	FFFO
Sense	Local
Interface	Memory-Mapped

CHAPTER 4

SETUP AND CONFIGURATION

Note: Refer to Appendix F for Wire Wrap Summary.
Refer to Appendix G for Wire Wrap, Component and Accessory Locations.

4.1 RTI-1260 SETUP AND CONFIGURATION

4.1.1 INPUT MULTIPLEXER CONFIGURATIONS

The RTI-1260 can be configured for either single-ended, differential or pseudo-differential inputs. The choice will depend upon the application. Reference Appendix A for applications information on these configurations. Reference Appendix B for applications information on 4-20mA current inputs.

The multiplexer inputs are configured by wire wrap jumpers as shown in Table 4.

Configuration	Jumper	Channel Capacity STD	Channel Capacity Expanded (Using OA10)
Single-Ended	34 to 37 to 41 35 to 36	16	32
Differential	30 to 31 34 to 41 35 to 37	8	16
Pseudo-Differential	34 to 37 to 41 35 to 42	16	32

Table 4.1 Input Multiplexer Selection

Channel Expansion–The channel capacity on the RTI-1260 can be increased for 16 SE/8 DIFF channels to 32 SE/16 DIFF with the additional two multiplexer ICs (ADI PIN OA10).

Warning–These components are CMOS and proper handling procedures should be used.

Insertion–Insert in sockets labeled Z3 and Z4 with orientation identical to multiplexers in positions Z1 and Z2.

4.1.2 SETTING PGA GAIN

The resistor programmable gain amplifier (PGA) allows the user to amplify low level input signal to the full scale input range of the A/D converter. This is accomplished with the use of a single resistor.

An example of using the PGAs gain is shown in Figure 4.1.

Setting the gain of the PGA is accomplished by installing a single resistor. This resistor should be a high-stability metal film type (RN55 style, ±25ppm/°C typ). The relationship between the gain-setting resistor RG1 and the resultant gain (G) is $R_G = \frac{20k\Omega}{G-1}$

Fine adjustment of the gain can be accomplished using the ADC gain, R20 or by the addition of a large value resistor (RG2) which is in parallel with RG1.

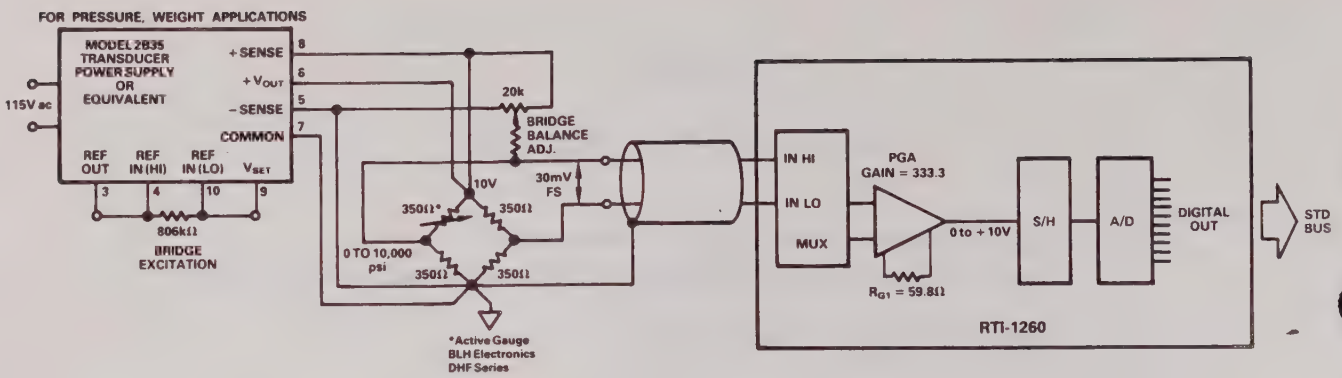


Figure 4.1 Strain Gage Example

4.1.2.1 A/D CONVERSION DELAY

The conversion delay circuit provides a delay from the time a multiplexer channel is selected and the time an A/D conversion takes place. It prevents a conversion to take place before the multiplexer and S/H have settled. This delay, typically 15μs must be increased when higher gain ranges are used. Refer to Table 4.2 to select the appropriate value of CT.

Selected Gain	Recommended CT Value	Conversion Delay (microseconds) (Settle to ±1LSB)
1—150	Open	13
151—300	680pF	21
301—500	1500pF	28
501—700	3300pF	40
701—1000	6200pF	85

Table 4.2 CT Value vs. Gain

4.1.3 A/D INPUT RANGE SELECTION

The available A/D input ranges and the wire wrap connections necessary to obtain them are listed in Table 4.3.

Input Range	Output Code	Jumper
0 to +10V	Straight Binary	28 to 29 38 to 40
±10V	Offset Binary or 2's Complement	27 to 29 39 to 40

Table 4.3 Analog Input Range Selection

Refer to Appendix E for the listing of analog values vs. digital codes.

4.1.4 A/D OUTPUT CODE SELECTION

The output of the A/D is a digital word presented on command to the microcomputer data bus. Three codes can be selected by wire wrap jumpers listed in Table 4.4.

A/D Output Code	Jumper
Straight Binary	19 to 20 22 to 23
Offset Binary	19 to 20 22 to 23
2's Complement	20 to 21 23 to 24

Table 4.4 Analog Output Code Selection

4.1.5 INTERFACE MODE SELECTION

The RTI-1260 can interface as a memory-mapped or port-mapped device to the STD bus. It can also map in the normal or extended memory or I/O space using $\overline{\text{MEMEX}}$ or $\overline{\text{IOEX}}$. It can also be jumpered to ignore $\overline{\text{MEMEX}}$ or $\overline{\text{IOEX}}$ which is necessary if the user is performing special functions with these lines.

Memory Mapped I/O	
Normal Memory	48–50, 51–52, 44–45
Extended Memory	48–50, 51–52, 44–55, 45–54
Ignore $\overline{\text{MEMEX}}$	48–50, 51–52, 45–46
Port-Mapped I/O	
Normal Port Image	49–50, 52–53, 45–47
Extended Port Image	49–50, 52–53, 47–55, 45–54
Ignore $\overline{\text{IOEX}}$	49–50, 52–53, 45–46

Note: Pins 43 and 45 are same node.

Table 4.5 RTI-1260 Interface Mode Selection

4.1.6 BASE ADDRESS SELECTION

The base address of memory or I/O space is selected by wire wrap jumpers as shown in Table 4.6. The RTI-1260 must be positioned in an unoccupied location. See section 5.2 for the maps.

The memory-mapped base address will be XFY0 where X and Y are selected in Table 4.6. The I/O port-mapped base address will be Y0 where Y is selected in Table 4.6. The board will occupy 16 consecutive bytes of memory or I/O ports.

Base Address	X Digit Jumpers				Y Digit Jumpers			
Hex Digit	5–6	13–14	11–12	3–4	7–8	15–16	9–10	1–2
0	*	*	*	*	*	*	*	*
1	*	*	*		*	*	*	
2	*	*		*	*	*		*
3	*	*			*	*		
4	*		*	*	*		*	*
5	*		*		*		*	
6	*			*	*			*
7	*				*			
8		*	*	*		*	*	*
9		*	*			*	*	
A		*		*		*		*
B		*				*		
C			*	*			*	*
D			*				*	
E				*				*
F								
Address Bit	A15	A14	A13	A12	A7	A6	A5	A4

Note: Install jumpers between posts indicated by asterisk for address digit desired.

Table 4.6 Base Address Selection

Example

To select memory base address BF70, jumper 13 to 14 and 7 to 8.

4.1.7 SYSTEM RESET

This signal is connected to provide an initialization of the card on power turn on, etc. Whenever a reset signal is received the following events will occur:

1. The Busy signal on bit 7 of XFYD will be cleared to zero.
2. The Multiplexer will be reset to its first channel (00).

4.1.8 EXTERNAL CONVERT COMMAND

In this mode of operation, the A/D converter can be started by an external command which is applied between wire wrap pins 25 and 26. Once a desired multiplexer channel is selected, conversions are initiated by an external source of TTL compatible pulses. After the initial settling time of the selected channel, there is no delay between command and the start of the conversion (see Figure 4.2). This mode is useful in collecting a sequence of data samples from the same channel at precise time intervals as required in signal analysis or for synchronizing the conversion with external events.

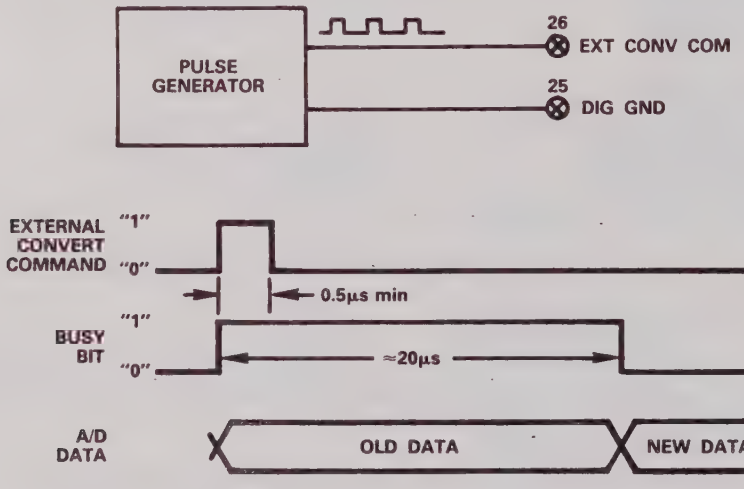


Figure 4.2 External Convert Command Timing Diagram

4.2 RTI-1262 SETUP AND CONFIGURATION

4.2.1 D/A INPUT CODE SELECTION

The available D/A input codes are determined by the selected analog output range. Table 4.7 gives the relationship between digital input code and analog output range.

Input Code	Output Code
Straight Binary	0 to +5V, 0 to +10V (unipolar)
Offset Binary	0 to ±5V, 0 to ±10V (bipolar)

Table 4.7 Digital Input Code Selection

Refer to Appendix E for a listing of analog values vs. digital codes.

4.2.2 D/A OUTPUT VOLTAGE RANGE SELECTION

The output of the D/A is an analog value equivalent to the digital word written on the digital input. Four output ranges can be selected by wire wrap jumpers listed in Table 4.8.

D/A	Output Range	Jumper
DAC0	0 to +5V	36 to 38 17 to 18 (open)
	0 to +10V	37 to 38 17 to 18 (open)
	±5V	36 to 38 17 to 18
	±10V	37 to 38 17 to 18
DAC1	0 to +5	39 to 41 19 to 20 (open)
	0 to +10V	40 to 41 19 to 20 (open)
	±5V	39 to 41 19 to 20
	±10V	40 to 41 19 to 20
DAC2	0 to +5V	42 to 44 21 to 22 (open)
	0 to +10V	43 to 44 21 to 22 (open)
	±5V	42 to 44 21 to 22
	±10V	43 to 44 21 to 22
DAC3	0 to +5V	45 to 47 48 to 49 (open)
	0 to +10V	46 to 47 48 to 49 (open)
	±5V	45 to 47 48 to 49
	±10V	46 to 47 48 to 49

Table 4.8 Analog Output Range Selection

The RTI-1262 can interface as a memory-mapped or port-mapped device to the STD bus. It can also map in the normal or extended memory or I/O space using $\overline{\text{MEMEX}}$ or $\overline{\text{IOEX}}$. It can also be jumpered to ignore $\overline{\text{MEMEX}}$ or $\overline{\text{IOEX}}$ which is necessary if the user is performing special functions with these lines.

Memory Mapped I/O	
Normal Memory	58–60, 55–56, 51–52
Extended Memory	58–60, 55–56, 51–61, 52–62
Ignore $\overline{\text{MEMEX}}$	58–60, 55–56, 52–54
Port-Mapped I/O	
Normal Port Image	59–60, 56–57, 52–53
Extended Port Image	59–60, 56–57, 53–61, 52–62
Ignore $\overline{\text{IOEX}}$	59–60, 56–57, 52–54

Note: Pins 50 and 52 are same node.

Table 4.9 RTI-1262 Interface Mode Selection

4.2.4 BASE ADDRESS SELECTION

The base address of memory or I/O space is selected by wire wrap jumpers as shown in Table 4.9. The RTI-1262 must be positioned in an unoccupied location. See section 5.3 for the maps.

The memory-mapped base address will be XFY0 where X and Y are selected in Table 4.9. The I/O port-mapped base address will be Y0 where Y is selected in Table 4.9. The board will occupy 16 consecutive bytes of memory or I/O ports.

Base Address	X Digit Jumpers				Y Digit Jumpers			
Hex Digit	5–6	13–14	11–12	3–4	7–8	15–16	9–10	1–2
0	*	*	*	*	*	*	*	*
1	*	*	*		*	*	*	
2	*	*		*	*	*		*
3	*	*			*	*		
4	*		*	*	*		*	*
5	*		*		*		*	
6	*			*	*			*
7	*				*			
8		*	*	*		*	*	*
9		*	*			*	*	
A		*		*		*		*
B		*				*		
C			*	*			*	*
D			*				*	
E				*				*
F								
Address Bit	A15	A14	A13	A12	A7	A6	A5	A4

Note: Install jumpers between posts indicated by asterisk for address digit desired.

Figure 4.9 RTI-1262 Base Address Selection

Example

To select memory base address BF70, jumper 13 to 14 and 7 to 8.

4.2.4.1 OPTIONAL MAP LOCATION

This feature offsets the base address by 8 bytes and allows two RTI-1262s to occupy the same 16 bytes. Table 4.10 gives the wire wrap jumper positions to enable this function. Figure 5.3 lists the new locations.

Memory Map	Jumper
Standard	24 to 25
Optional	23 to 24

Table 4.10 Optional Memory Map

4.2.5 CONFIGURING 4-20mA CURRENT LOOP OUTPUTS (OPTION)

Two D/A outputs (DAC0 and DAC1) can be configured for 4-20mA outputs. This is accomplished by soldering the OA08 V/I converter into the appropriate (M2 for DAC0 and M3 for DAC1). The 4-20mA hookup is shown in Figure 4.3.

Note: When using the 4-20mA option, the D/A output must be configured for 0 to +10V.

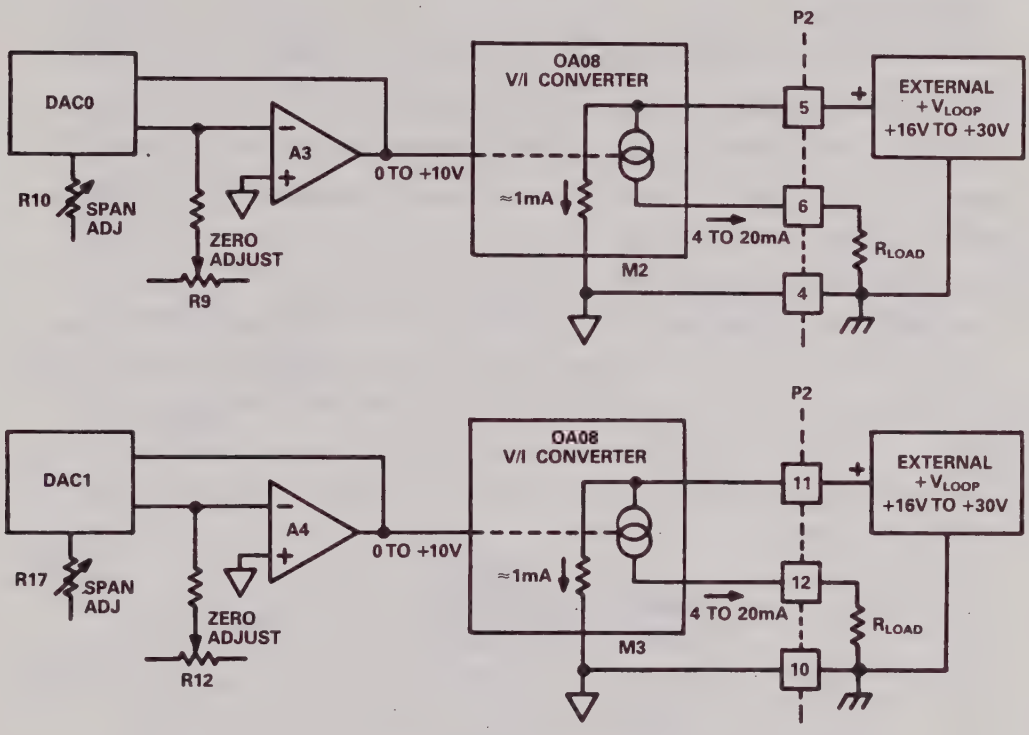


Figure 4.3 4-20mA Hookup

The current loop outputs meet all requirements of ISA-S50.1 for Type 3, Class L, nonisolated 4-20mA current loop transmitters. The output current in each loop is proportional to the value of the digital word presented to the selected D/A converter. The relationship between the digital input word and the analog output current is given by: I = 4.00mA + 16.00mA × D/4096 where I is the output current in mA and D is the decimal expression to the digital word.

There is no minimum resistance for the loads driven by the current loops; they can drive even a short circuit with no loss of linearity and with no damage to the unit. The *maximum* resistance of the load as seen by the current loop drivers (that is, the total resistance of the load or loads and the interconnecting wire) is limited, however. The constraining factor is that the voltage appearing between I_{OUT} and analog common should not exceed +10V. (Exceeding a +10V output will not damage the unit, but clipping of the signal will result.) The maximum total resistance of the loop is, therefore, 10V/I max. Usually I max will be the full-scale output of 20mA, making the maximum load equal to 10V/20mA = 500 ohms. Many devices used with 4-20mA transmitters have a load resistance of 250 ohms; in those cases, the interconnecting wire could have up to an additional 250 ohms of resistance.

Power for the current loop outputs can be derived from a power supply located at the load or at the driving end of the cable. It should be noted that the full +10V output voltage capability of the current loop outputs is available only if the loop power supply is +16V minimum. Operation from a +15V supply will reduce the maximum output voltage to +9V. The maximum permissible loop supply voltage is +30V.

4.2.6 SYSTEM RESET

This signal is connected to provide an initialization of the card on power on, etc.

Whenever a reset signal is received, the following events will occur;

1. The DAC input data registers and buffer registers will be cleared to zero.

Note that this results in an initial zero volt output if strapped for unipolar mode and a −FS output if strapped for bipolar.

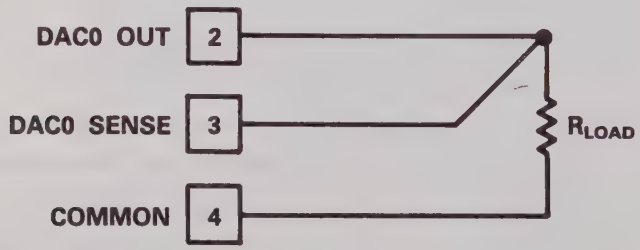
4.2.7 USING D/A SENSE LINES

A voltage drop occurs between the RTI-1262 output and the load, resulting in an error. This line loss can be eliminated by connecting the SENSE at the load. This method is referred to as Remote Sensing and can eliminate up to 3 volts of line loss.

If the application is such that Remote Sensing is not required, jumpers should be installed as follows.

D/A	Jumper
DAC0	28 to 29
DAC1	30 to 31
DAC2	32 to 33
DAC3	34 to 35

For Remote Sensing, these jumpers are not connected and the D/A connection on P2 is wired to the load as follows.



CHAPTER 5

PROGRAMMING AND OPERATION

5.1 INTRODUCTION

This section contains the information necessary to write effective software for analog input and output using the RTI-1260 and RTI-1262.

It is assumed that the reader is familiar with assembly language programming. The program example in this user's guide uses 8085 code, however Z-80 or 6800 code could have been used.

The RTI card interfaces to the STD system as a block of 16 contiguous bytes of memory or I/O ports. If the RTI is treated as a block of memory, simple memory read and write instructions are used. If used as I/O ports, input and output instructions are used.

5.2 RTI-1260 MAP

The RTI-1260 uses 3 of the 16-bytes which are assigned as follows.

BYTE ADDR.	DATA FORMAT								FUNCTION	OPER.
	D7	D6	D5	D4	D3	D2	D1	D0		
XFYB	ϕ	ϕ	ϕ	M_4	M_3	M_2	M_1	M_0	MUX ADDR/ CONV	WRITE
XFYC	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	A/D DATA LO	READ
XFYD	BUSY	0 / MSB	0 / MSB	0 / MSB	MSB / MSB	B_{10}	B_9	B_8	A/D DATA HI	READ

NOTES:
1. **X AND Y ARE USER SELECTABLE.**
2. **BITS SHOWN AS [ ] HAVE THE UPPER VALUE FOR UNIPOLAR CODES AND LOWER VALUE FOR 2's COMPLEMENT.**
3. **THE SYMBOL ϕ MEANS THE BITS IS IGNORED.**
4. **BUSY BIT EQUALS "1" DURING CONVERSIONS AND "0" WHEN DONE.**
5. **ONLY YB, YC AND YD ARE USED FOR I/O PORTS. (LOWER 8 ADDRESS BITS)**

Figure 5.1 RTI-1260 Map

MUX ADDRESS/CONV

Any random input channel can be selected by writing the channel code into bits D0 to D4 of this byte. The channel address can range from 00000 to 11111 binary (0 to 31 decimal) for 32 single ended input channels and 00000 to 01111 for 16 differential channels. Writing to the byte will also initiate an A/D conversion.

A/D DATA HI

The BUSY bit is used to indicate when an ADC conversion is complete, resulting in valid A/D data. This bit is a "1" when busy and a "0" when complete.

The 4 highest order bits of the A/D are also available at this address. If the A/D has been set up for 2's complement, bipolar coding, then D6, D5, D4 and D3 will read the $\overline{\text{MSB}}$ (inverted MSB).

A/D DATA LO

The 8 lowest order bits of the A/D are available at this address.

5.3 RTI-1262 MAP

The RTI-1262 uses 8 of the 16 contiguous bytes which are assigned as follows:

BYTE ADDR.	DATA FORMAT D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	OPER.
XFY0	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	D/A DATA 0 LO	WRITE
XFY1	ϕ	ϕ	ϕ	ϕ	MSB	B_{10}	B_9	B_8	D/A DATA 0 HI	WRITE
XFY2	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	D/A DATA 1 LO	WRITE
XFY3	ϕ	ϕ	ϕ	ϕ	MSB	B_{10}	B_9	B_8	D/A DATA 1 HI	WRITE
XFY4	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	D/A DATA 2 LO	WRITE
XFY5	ϕ	ϕ	ϕ	ϕ	MSB	B_{10}	B_9	B_8	D/A DATA 2 HI	WRITE
XFY6	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	D/A DATA 3 LO	WRITE
XFY7	ϕ	ϕ	ϕ	ϕ	MSB	B_{10}	B_9	B_8	D/A DATA 3 HI	WRITE

NOTES: 1. X AND Y ARE USER SELECTABLE.
2. THE SYMBOL ϕ MEANS THE BIT IS IGNORED.
3. ONLY LOWER 8 ADDRESS BITS USED FOR I/O PORTS.

Figure 5.2 RTI-1262 Map

D/A DATA

Two bytes are assigned to each of the 4 analog output channels. The digital data is written for each D/A with the lower address byte containing the 8 least significant bits and the next higher address byte containing the 4 most significant bits. The D/A data is double buffered on the RTI card so that the data for both bytes are loaded into the D/A when the DAC HI BYTE written to, therefore ensuring a one step update of the D/A output.

5.3.1 RTI-1262 OPTIONAL MAP LOCATION

The RTI-1260 and RTI-1262 can occupy the same 16 byte block when using this option. The new RTI-1262 map is shown in Figure 5.3. (See section 4.2.4.1 for details).

BYTE ADDR.	DATA FORMAT D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION	OPER.
XFY8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	D/A DATA 0 LO	WRITE
XFY9	ϕ	ϕ	ϕ	ϕ	MSB	B_{10}	B_9	B_8	D/A DATA 0 HI	WRITE
XFYA	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	D/A DATA 1 LO	WRITE
XFYB	ϕ	ϕ	ϕ	ϕ	MSB	B_{10}	B_9	B_8	D/A DATA 1 HI	WRITE
XFYC	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	D/A DATA 2 LO	WRITE
XFYD	ϕ	ϕ	ϕ	ϕ	MSB	B_{10}	B_9	B_8	D/A DATA 2 HI	WRITE
XFYE	B_7	B_6	B_5	B_4	B_3	B_2	B_1	LSB	D/A DATA 3 LO	WRITE
XFYF	ϕ	ϕ	ϕ	ϕ	MSB	B_{10}	B_9	B_8	D/A DATA 3 HI	WRITE

NOTES: 1. X AND Y ARE USER SELECTABLE.
2. THE SYMBOL ϕ MEANS THE BIT IS IGNORED.
3. ONLY LOWER 8 ADDRESS BITS USED FOR I/O PORTS.

Figure 5.3 RTI-1262 Map (optional)

5.4 BASIC A/D CONVERSION (Assuming Memory-Mapped Interface)

The basic A/D data acquisition function is to acquire a single reading from a single channel. When using the RTI-1260 card, a conversion occurs for every write to the multiplexer address byte.

If we use the following labels;

```
MUXCV   EQU   XFYBH
ADCHI   EQU   XFYDH
ADCLO   EQU   XFYCH
```

where X and Y are determined by the selected memory location of the card.

The program below will perform this transfer.

```
        MVI   A,07H
        STA   MUXCV     ; SELECT CH07 AND START CONVERT
                          (Busy Bit goes to "1")
TEST:   LDA   ADCHI
        RLC
        JC    TEST      ; CHECK BUSY BIT
        LHLD  ADCLO     ; READ DATA
```

In this example, the multiplexer address is set at 07 and the BUSY bit goes to a "1", 15μs (typ) after written to this MUX ADR/CONV byte. The program then goes into a loop where the BUSY bit is tested to see if the conversion is complete. When the conversion is complete, BUSY equal "0", the A/D data is read and stored in register pain H and L.

5.5 BASIC D/A CONVERSION (Assuming Memory-Mapped Interface)

The RTI-1262 is used to convert 12 bits of digital data into an analog output signal. A two byte transfer is required to interface the 8-bit STD data bus to the 12-bit D/A. A buffer register is provided on the card so that the D/A is updated in one step.

If we use the following labels

```
DA0LO    EQU    XFY0H
DA1LO    EQU    XFY2H
DA2LO    EQU    XFY4H
DA3LO    EQU    XFY6H
```

where X and Y are determined by the selected memory location of the card.

The program below writes data into the D/A using a single instruction.

```
LXI     H, DATA     ; LOAD DATA
SHLD    DA1LO       ; TRANSFER TO D/A 1
```

In this example, the data in the H and L register pair is loaded into D/A 1.

CHAPTER 6

HOOKUP

6.1 RTI-1260 ANALOG INPUT CONNECTION (P2)

Connector P2 is used for the analog connection. The pin assignments are shown for the connector in Table 6.1.

The RTI-1260 card contains a 3M No. 3433 50-pin connector. Recommended mating connectors to P2 are listed below.

Manufacturer	P/N	Description
Analog Devices	AC1553	50-Pin Flat Cable Connector with 3'Color Coded Cable
3M	3425-0000	50-Pin Flat Cable Connector

1	CH0 (CH0 HIGH)	2	CH8 (CH0 LOW)
3	COMMON	4	CH9 (CH1 LOW)
5	CH1 (CH1 HIGH	6	COMMON
7	CH2 (CH2 HIGH)	8	CH10 (CH2 LOW)
9	COMMON	10	CH11 (CH3 LOW)
11	CH3 (CH3 HIGH)	12	COMMON
13	CH4 (CH4 HIGH)	14	CH12 (CH4 LOW)
15	COMMON	16	CH13 (CH5 LOW)
17	CH5 (CH5 HIGH)	18	COMMON
19	CH6 (CH6 HIGH)	20	CH14 (CH6 LOW)
21	COMMON	22	CH15 (CH7 LOW)
23	CH7 (CH7 HIGH)	24	COMMON
25	CH16 (CH8 HIGH)	26	CH24 (CH8 LOW)
27	COMMON	28	CH25 (CH9 LOW)
29	CH17 (CH9 HIGH)	30	COMMON
31	CH18 (CH10 HIGH)	32	CH26 (CH10 LOW)
33	COMMON	34	CH27 (CH11 LOW)
35	CH19 (CH11 HIGH)	36	COMMON
37	CH20 (CH12 HIGH)	38	CH28 (CH12 LOW)
39	COMMON	40	CH29 (CH13 LOW)
41	CH21 (CH13 HIGH)	42	COMMON
43	CH22 (CH14 HIGH)	44	CH30 (CH14 LOW)
45	COMMON	46	CH31 (CH15 LOW)
47	CH23 (CH15 HIGH)	48	COMMON
49	P.D. SENSE	50	COMMON

Note: Parenthesis indicates pin assignments for differential mode.

Table 6.1 RTI-1260 P2 Connections

6.2 RTI-1262 ANALOG OUTPUT CONNECTION (P2)

Connector P2 is used for the analog connection. The pin assignments are shown for the connector in Table 6.2.

The RTI-1262 card contains a 3M No. 3429 26-pin connector. Recommended mating connectors to P2 are listed below.

Manufacturer	P/N	Description
Analog Devices	AC1554	26-Pin Flat Cable Connector with 3'Color Coded Cable
3M	3399-0000	26-Pin Flat Cable Connector

1	COMMON	2	DAC 0 OUT
3	DAC 0 SENSE	4	COMMON
5	DAC 0 LOOP POWER	6	DAC 0 CURRENT OUT
7	COMMON	8	DAC 1 OUT
9	DAC 1 SENSE	10	COMMON
11	DAC 1 LOOP POWER	12	DAC 1 CURRENT OUT
13	COMMON	14	DAC 2 OUT
15	DAC 2 SENSE	16	COMMON
17	N/C*	18	N/C*
19	COMMON	20	DAC 3 OUT
21	DAC 3 SENSE	22	COMMON
23	N/C*	24	N/C*
25	COMMON	26	COMMON

*N/C = No Connection

Table 6.2 RTI-1262 P2 Connections

CHAPTER 7

CALIBRATION

The RTI-1260 series are calibrated to the specified accuracy at the factory, however, it may be desirable to check and trim the calibration after the boards are set up and running in the system backplane.
The following equipment will be required:

1. Voltmeter with 1/2LSB resolution and accuracy (2.5mV for ±10V range at G = 1). Fluke Model 8200 A, Hewlett-Packard Model 3466 A or equivalent.
2. Low Noise Voltage Source for analog input or external reference calibration (adjustable over ±10V range). Fluke Model 515A, Hewlett-Packard Model 382 A or equivalent.

7.1 RTI-1260 CALIBRATION PROCEDURES

1. Disconnect analog card inputs and connect the voltage source. Apply the proper calibration voltage for zero adjustment to the selected input channel.
2. The ADC data from a conversion should be 0000_{16} Binary Code or 0800_{16} Two's Complement Code. With the converter performing repetitive conversions on the selected channel, adjust the zero potentiometer (R21) so that the LSB of the output jitters between 1 and 0 and then rotate the R21 trim pot just enough so that the LSB stabilizes to 0. This sets the offset or zero of the ADC.
3. Apply the proper full scale calibration voltage for gain adjustment to the selected input channel.
4. The ADC data after a conversion should be $0FFF_{16}$ Binary Code or $07FF_{16}$ Two's Complement Code. With the ADC performing repetitive conversions, adjust the gain potentiometer (R20) so that the LSB jitters between 0 and 1. Then rotate the potentiometer (R20) just enough so that the LSB stablizes at 1. This sets the full scale of the ADC and the input section is now calibrated.

	Scale Points	
	Zero	Gain
ADC Input Ranges @ G = 1	**(−FS +1/2LSB)**	**(+FS −1 1/2LSB)**
0V to +10V	+1.22mV	+9.9963V
−10V to +10V	−9.9976V	+9.9927V

Table 7.1 RTI-1260 Calibration Voltage

7.2 RTI-1262 CALIBRATION

7.2.1 D/A VOLTAGE OUTPUT

The D/A converters only require one input code change per set point. The voltmeter is to be used to read the analog output as adjustments are being made.

1. First, write, the negative full scale code to each DAC, 0000_{16}.

2. Adjust the zero potentiometer (R5 for DAC 0, R12 for DAC 1, R19 for DAC 2, R26 for DAC 3) for the proper analog output according to the table below.
3. Next, write the positive full scale code to each DAC-OFFF$_{16}$.
4. Adjust the gain potentiometer (R10 for DAC 0, R17 for DAC 1, R24 for DAC 2, R31 for DAC 3) for the proper analog output according to the table below.
5. The D/A converters are now calibrated properly.

	Scale Points	
	Zero	Gain
DAC Output Range	**(−FS)**	**(+FS − 1LSB)**
0V to +5V	0.0000V	+4.9988V
0V to +10V	0.0000V	+9.9988V
−5V to +5V	−5.0000V	+4.9976V
−10V to +110V	−10.0000V	+9.9951V

Table 7.2 RTI-1262 Calibration Voltage

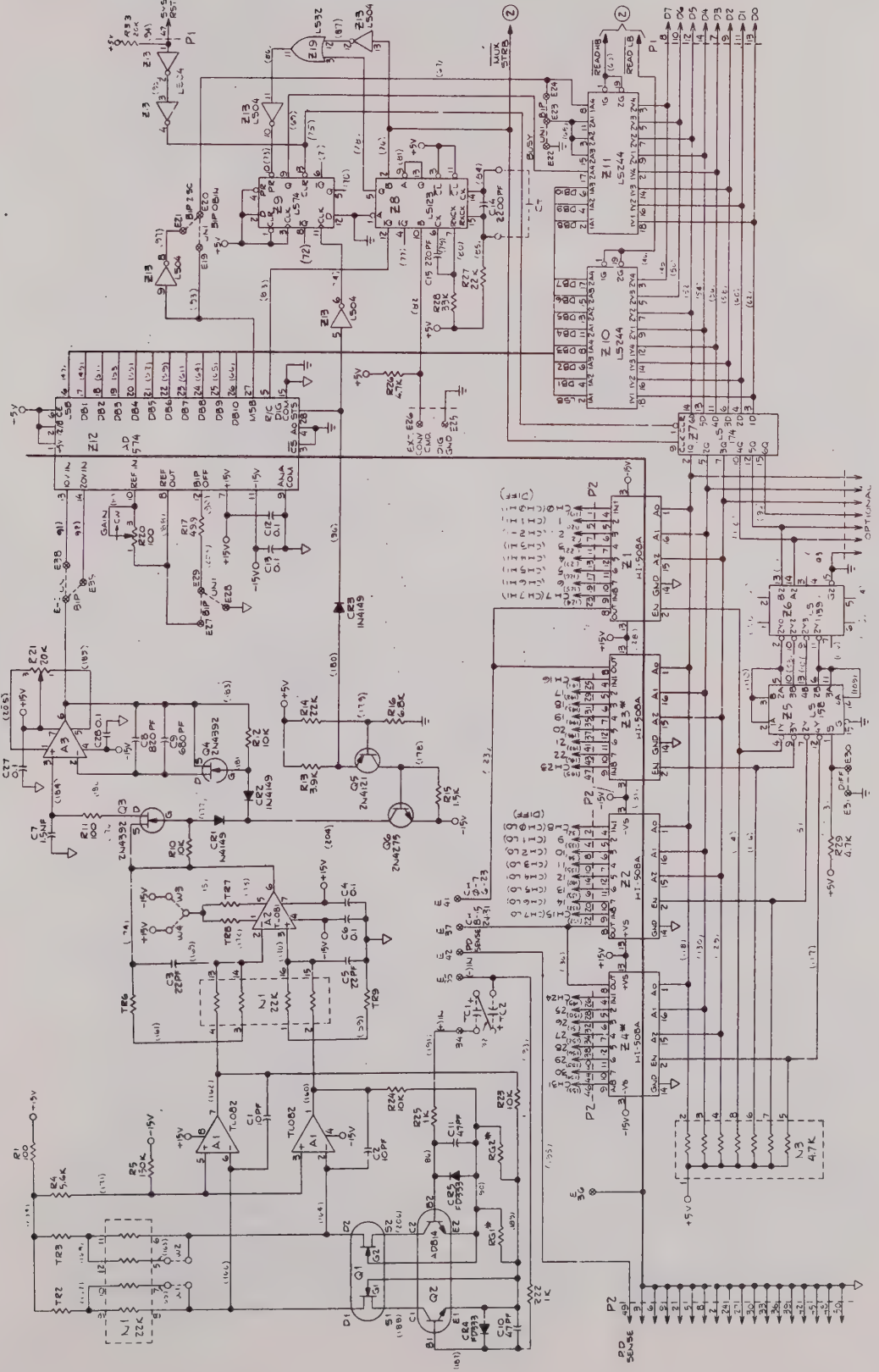
7.2.2 CURRENT LOOP OUTPUT CALIBRATION PROCEDURES

The V to I Converter will work only with an input of 0 to +10V so the associated DAC must be connected for unipolar output mode when current loop output is desired. After the loop has been connected, calibration is performed using the zero and gain adjustment potentiometers of the associated DAC as follows:

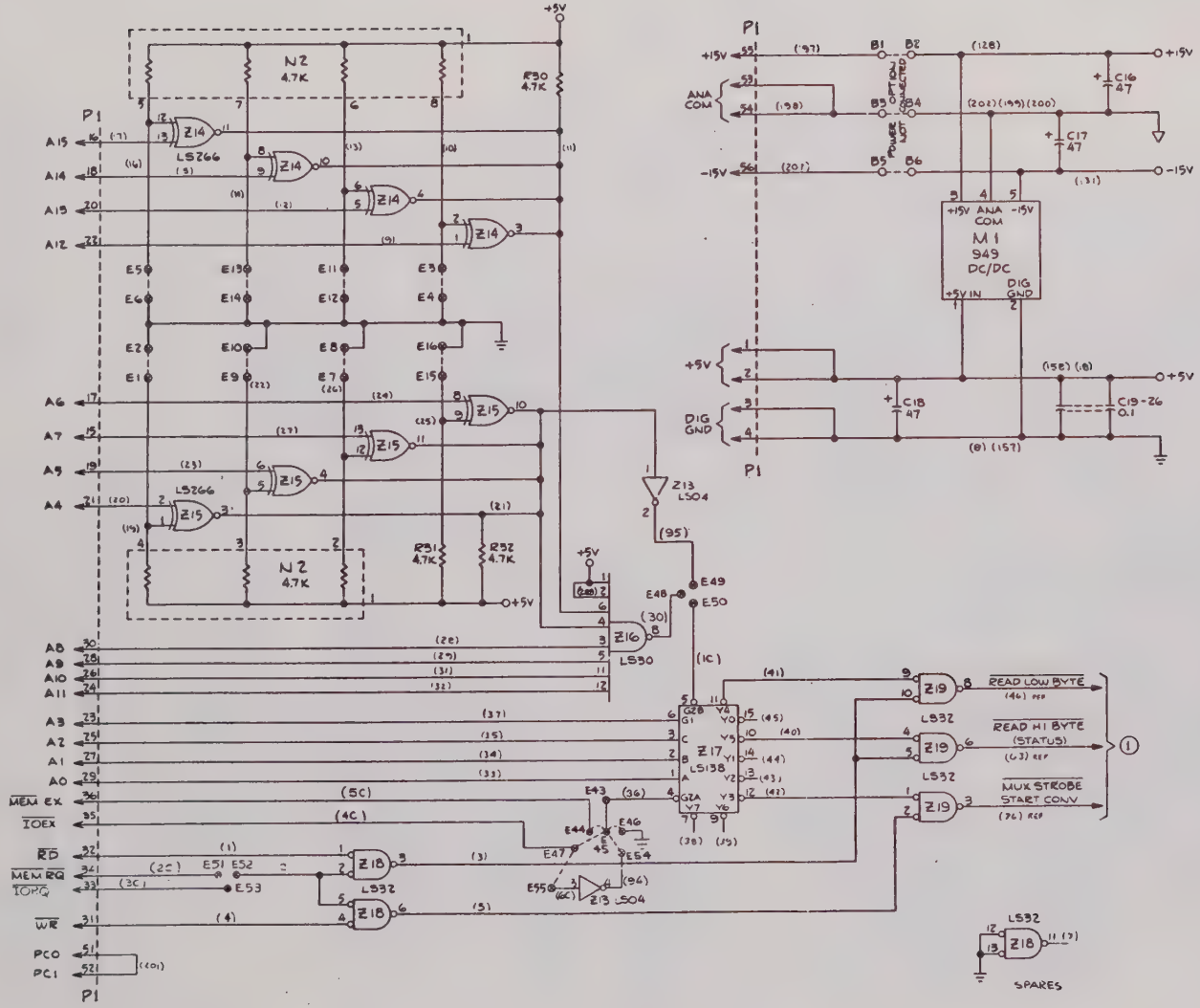
1. Connect the voltmeter across the load resistor.
2. Write the zero code to the DAC (0000_{16}).
3. Adjust the ZERO pot (R5 for DAC 0, R12 for DAC 1) for a reading on the voltmeter corresponding to exactly 4.000mA flowing through the load resistor.
4. Write the full scale code to the DAC (FFF_{16}).
5. Adjust the GAIN pot (R10 for DAC 0, R17 for DAC 1) for a voltage across the load corresponding to a current of 20.000mA −1LSB or 19.961mA through the load.

   Note: While the output of the associated DAC will still be nominally 0 to +10V and be available simultaneously with the current output, this voltage output may not be accurate to 12 bits after adjustments are made to trim the current loop output.

APPENDIX A
RTI-1260 SCHEMATIC



RTI-1260 Schematic Diagram
Sheet 1
**Optional Components*

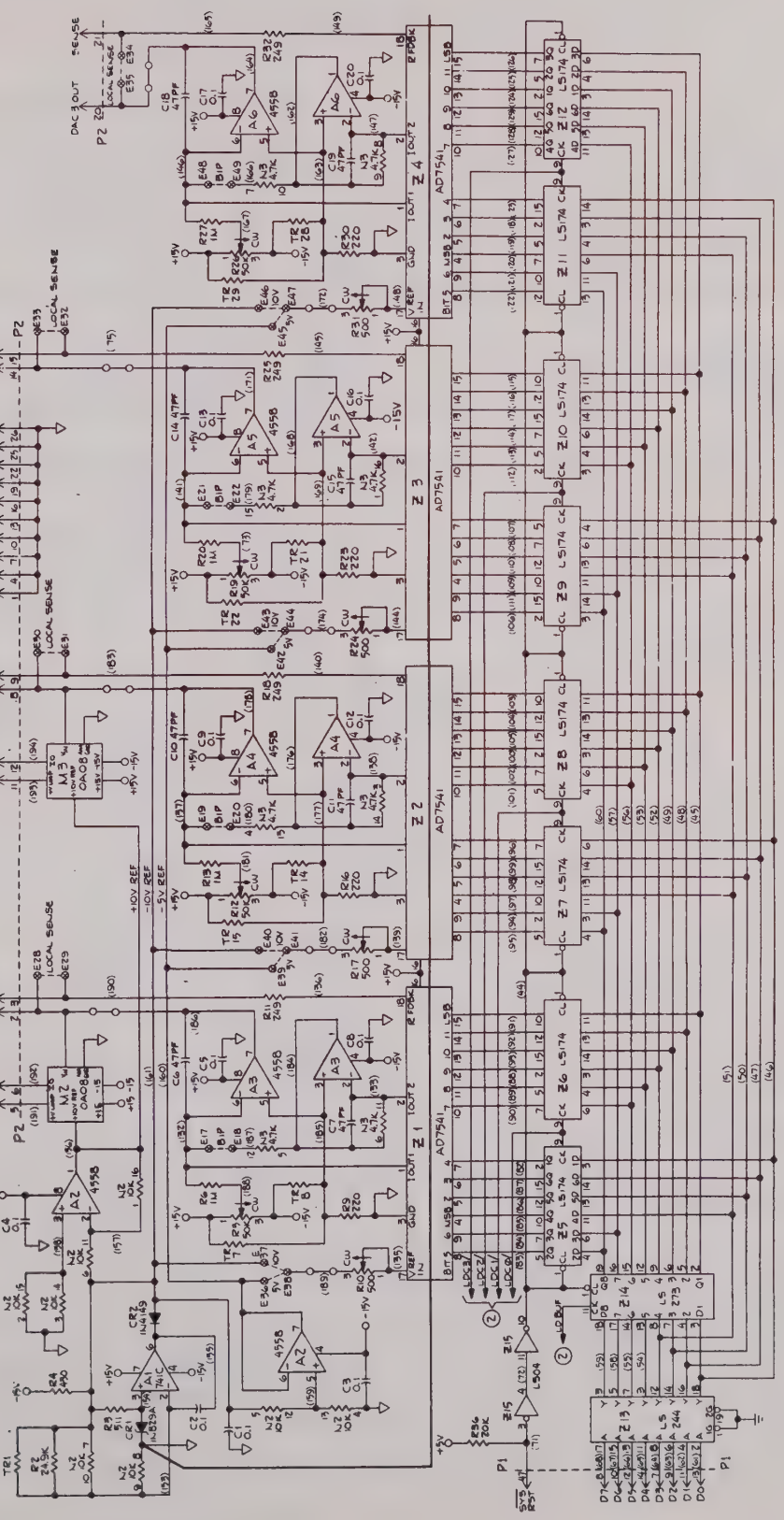


NOTES:

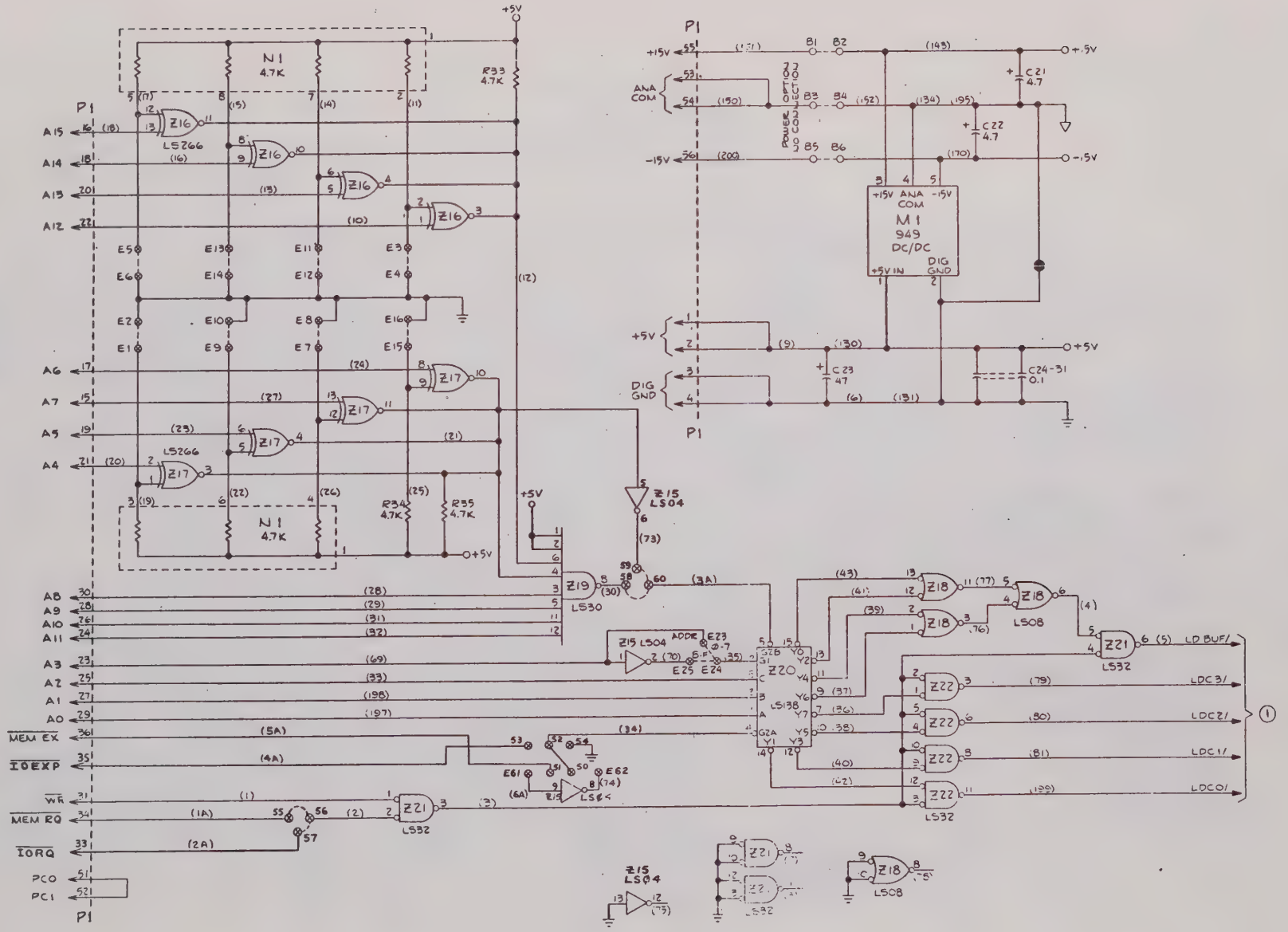
1. # Z3 & Z4 ARE OPTIONAL COMPONENTS.
2. W3 IS INSTALLED AT ASS'Y.
3. +5V: PIN 14, Z9 13 14 15 16 18,19.
   PIN 16, Z5 6,7,8,17
   PIN 20, Z10, 11.
   GND: PIN 7 Z9 13 14 15 16 18 19
   PIN 8 Z5 6 7 8 17.
   PIN 10 Z10, 11
4. (2) INDICATES SIGNAL CONTINUED TO NEXT SHEET.
5. RG1, RG2 TC1, TC2 AND CT ARE CUSTOMER INSTALLED.

RTI-1260 Schematic Diagram
Sheet 2

APPENDIX B
RTI-1262 SCHEMATIC



RTI-1262 Schematic Diagram
Sheet 1
**Optional Components*



RTI-1262 Schematic Diagram
Sheet 2

APPENDIX C

VOLTAGE INPUT CONFIGURATIONS

INPUT MULTIPLEXER GUIDELINES

This RTI series product employs a very versatile data acquisition subsystem which can be user-configured for maximum effectiveness in a wide variety of applications. This section describes the choices available and provides all the information necessary to permit the user to tailor the data acquisition hardware to suit his own requirements. This section is concerned primarily with analog inputs and the microcomputer interface.

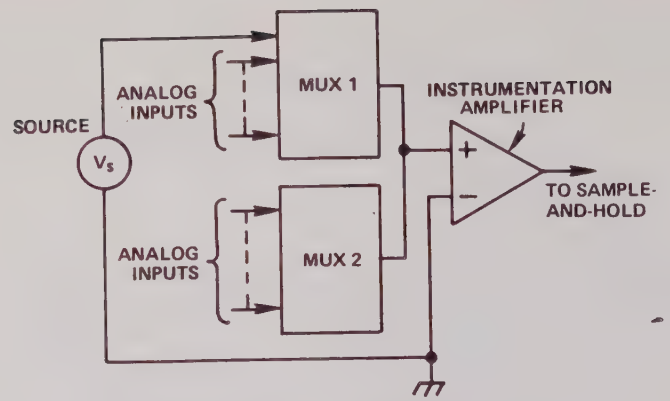
ANALOG INPUT MULTIPLEXER

As shown in Figure 1, there are three basic ways to configure the input multiplexer. The choice will depend upon the application, as described below.

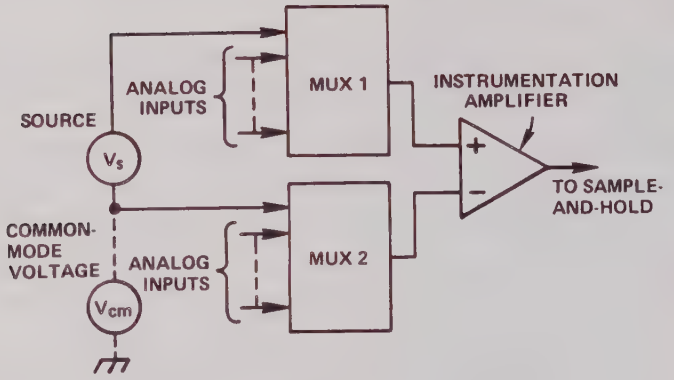
a. Single-Ended Input (Figure 1a) uses single-pole switching to select the desired input signal, and therefore, maximizes the available number of input channels. However, this configuration provides no rejection of common-mode noise and measures all inputs with respect to the local analog common. It is, therefore, best suited for use with relatively large signals (greater than 1 volt full scale) and in situations where the input signals originate close to the RTI card. Moreover, it is best used with low-impedance sources, since large source resistances will cause errors due to the instrumentation amplifier's input bias current.

b. Pseudo-Differential Input (Figure 1c) improves upon the single-ended scheme in one respect: it measures the input signals with respect to a common point at their source. It is still necessary that all signals have a common terminal, but the effects of voltage differences between the local common and the signal common are eliminated, and noise pickup in signal cables will be reduced to some extent. Thus, the signal sources can be farther from the multiplexer than would be desirable with single-ended operation, and the full complement of input channels is still available. Bias current errors will still exist if high source resistances are used. This input structure is useful in applications where it is necessary to reduce the effects of interchassis offsets, or other errors common to all input signals.

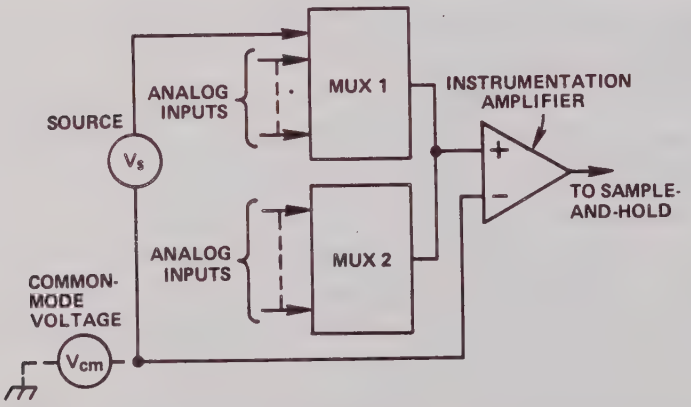
c. Full Differential Input (Figure 1b) is most effective in reducing the effects of noise and bias current, but sacrifices channel capacity. As shown in Figure 1c, a double-pole arrangement is used to switch both the high and low side of each signal source. Thus the input signals need not have a common point; each can "float" within the common-mode limits of the instrumentation amplifier. Common-mode noise voltages will be rejected by the instrumentation amplifier, and the symmetry of the input system will enhance ac noise rejection. If the source resistances seen at each lead of a signal pair are approximately equal, then error due to bias currents will tend to cancel, leaving only input offset current as an error source. Thus, full differential operation should be considered for any application involving low-level input signals, high source resistances, or significant amounts of common-mode noise, such as might result from long signal cables.



(a) Single-Ended



(b) Differential



(c) Pseudo-Differential

Figure 1. Input Multiplexer Configuration

In connection with full differential operation, it is important to remember that a return path must be provided for the input bias currents of the instrumentation amplifier. In cases where the signal source is floating (that is, it has no galvanic connection to the RTI card's analog common). a suitable path must be provided. Figure 2 shows how the signal cable shield can be used for this purpose.

Although the use of full differential multiplexing can minimize the effects of source resistance, system accuracy will generally be much better if large source resistances can be avoided. A signal with an effective resistance of 100 ohms will be quite vulnerable to noise contamination on even a short cable run, and above 10,000 ohms

the settling time of the input multiplexer will be degraded. Selection of the input multiplexer configuration on the RTI card is accomplished by means of wire-wrap jumpers.

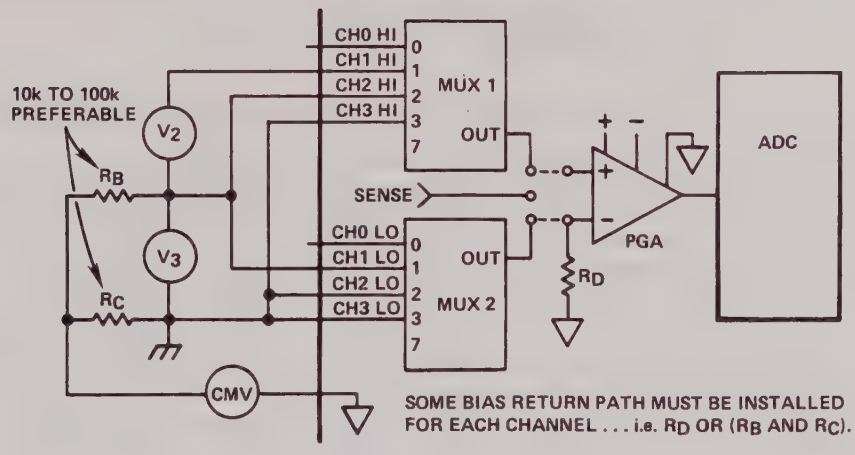


Figure 2.

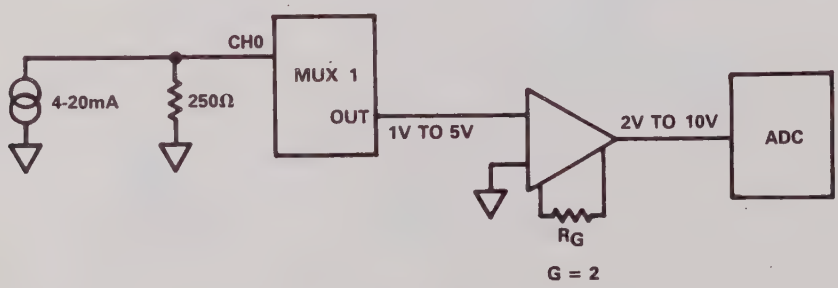
APPENDIX D

CURRENT LOOP INPUTS

The RTI card can be configured to directly accept the current loop signals (typically 4-20mA) used in process control system. When the single-ended configuration is chosen, one end of the load resistor is grounded, and it must, therefore, be the last load on the loop. Differential operation removes this restriction; other loads may be connected between the RTI's input and ground, provided that the common-mode input rate of the instrumentation amplifier is not exceeded. In most applications, the load resistor should be chosen to give a full-scale voltage of +5V or less, to keep power dissipation and loop voltage drop low. Thus, for a 4-20mA input signal, a 250 ohm resistor should be used, generating an input signal in the 1 to 5 volt range. Dale type RS-1/4W resistors are recommended for the purpose. To accommodate the resulting voltage signal, configure the A to D converter to the +10V range and operate the instrumentation amplifier at a gain of 2.

When the differential input mode is used and a large common-mode level is present due to other loads between the RTI and ground, it may be desirable to make the input swing smaller by using a smaller load resistor and a correspondingly higher gain.

Note that when using load resistors to convert 4-20mA current inputs to voltage in a single ended configuration, the return current for all loads is taken through the ground pins. When many load resistors are used, this current can be substantial, and it is advisable to provide a good ground to as many of the ground pins of the analog connector as possible.



Typical 4-20mA Input Configuration

APPENDIX E

ANALOG/DIGITAL CONVERSION TABLE

	±10.24V	±10V	±5.12V	±5V	±2.5V	Offset Binary	Two's Complement	Two's Comp/ OCTAL	Two's Comp/ HEX
+FS −1 LSB	+10.1395	+9.9951	+5.1175	+4.9976	+2.9988	1111 1111 1111	0111 1111 1111	003777	07FF
+3/4 FS	+7.6800	+7.5000	+3.8400	+3.7400	+1.8750	1110 0000 0000	0110 0000 0000	003000	0600
+1/2 FS	+5.1200	+5.0000	+2.5600	+2.5000	+1.2500	1100 0000 0000	0100 0000 0000	002000	0400
1/4 FS	+2.5600	+2.5000	+1.2800	+1.2500	+0.6250	1010 0000 0000	0010 0000 0000	001000	0200
0	0.0000	0.0000	0.0000	0.0000	0.0000	1000 0000 0000	0000 0000 0000	000000	0000
−1/4 FS	−2.5600	−2.5000	−1.2800	−1.2500	−0.6250	0110 0000 0000	1110 0000 0000	177000	0E00
−1/2 FS	−5.1200	−5.0000	−2.5600	−2.5000	−1.2500	0100 0000 0000	1100 0000 0000	176000	0C00
−3/4 FS	−7.6800	−7.5000	−3.8400	−3.7400	−1.8750	0010 0000 0000	1010 0000 0000	175000	0A00
−FS −LSB	−10.2395	−9.9951	−5.1175	−4.9976	−2.4988	0000 0000 0001	1000 0000 0001	174001	0801
−FS	−10.2400	−10.0000	−5.1200	−5.0000	−2.5000	0000 0000 0000	1000 0000 0000	174000	0800

12-Bit ADC Input vs. Output Table

Bit	Weight (of F.S.)	Summations (of F.S.)	Binary MSB		LSB
1	.5	.5	1000	0000	0000
2	.25	.75	1100	0000	0000
3	.125	.875	1110	0000	0000
4	.0625	.938	1111	0000	0000
5	.03125	.969	1111	1000	0000
6	.01562	.984	1111	1100	0000
7	.00781	.992	1111	1110	0000
8	.0039	.9961	1111	1111	0000
9	.00195	.9980	1111	1111	1100
10	.00097	.9990	1111	1111	1100
11	.00048	.99951	1111	1111	1110
12	.00024	.99976	1111	1111	1111

12-Bit ADC Bit Weights

APPENDIX F

RTI-1260 CONFIGURATION SUMMARY

MULTIPLEXER CONFIGURATION

Configuration	Jumper
Single-Ended	34 to 37 to 41 35 to 36
Differential	30 to 31 34 to 41 35 to 37
Pseudo-Differential	34 to 37 to 41 35 to 42

A/D INPUT RANGE

Input Range	Output Code	Jumper
0 to +10V	Straight Binary	28 to 29 38 to 40
±10V	Offset Binary or 2's Complement	27 to 29 39 to 40

A/D OUTPUT CODE

A/D Output Code	Jumper
Straight Binary	19 to 20 22 to 23
Offset Binary	19 to 20 22 to 23
2's Complement	20 to 21 23 to 24

INTERFACE MODE

Memory Mapped I/O

Normal Memory	48–50, 51–52, 44–45
Extended Memory	48–50, 51–52, 44–55, 45–54
Ignore $\overline{\text{MEMEX}}$	48–50, 51–52, 45–46

Port-Mapped I/O

Normal Port Image	49–50, 52–53, 45–47
Extended Port Image	49–50, 52–53, 47–55, 45–54
Ignore $\overline{\text{IOEX}}$	49–50, 52–53, 45–46

Note: Pins 43 and 45 are same node.

RTI-1262 CONFIGURATION SUMMARY

D/A OUTPUT RANGE

D/A	Output Range	Jumper
DAC0	0 to +5V	36 to 38 17 to 18 (open)
	0 to +10V	37 to 38 17 to 18 (open)
	±5V	36 to 38 17 to 18
	±10V	37 to 38 17 to 18
DAC1	0 to +5	39 to 41 19 to 20 (open)
	0 to +10V	40 to 41 19 to 20 (open)
	±5V	39 to 41 19 to 20
	±10V	40 to 41 19 to 20
DAC2	0 to +5V	42 to 44 21 to 22 (open)
	0 to +10V	43 to 44 21 to 22 (open)
	±5V	42 to 44 21 to 22
	±10V	43 to 44 21 to 22
DAC3	0 to +5V	45 to 47 48 to 49 (open)
	0 to +10V	46 to 47 48 to 49 (open)
	±5V	45 to 47 48 to 49
	±10V	46 to 47 48 to 49

OPTIONAL MAP LOCATION

Configuration	Jumper
Standard	24 to 25
Optional (Offset by 8 Bytes)	23 to 24

INTERFACE MODE

Memory Mapped I/O

Normal Memory	58–60, 55–56, 51–52
Extended Memory	58–60, 55–56, 51–61, 52–62
Ignore $\overline{\text{MEMEX}}$	58–60, 55–56, 52–54

Port-Mapped I/O

Normal Port Image	59–60, 56–57, 52–53
Extended Port Image	59–60, 56–57, 53–61, 52–62
Ignore $\overline{\text{IOEX}}$	59–60, 56–57, 52–54

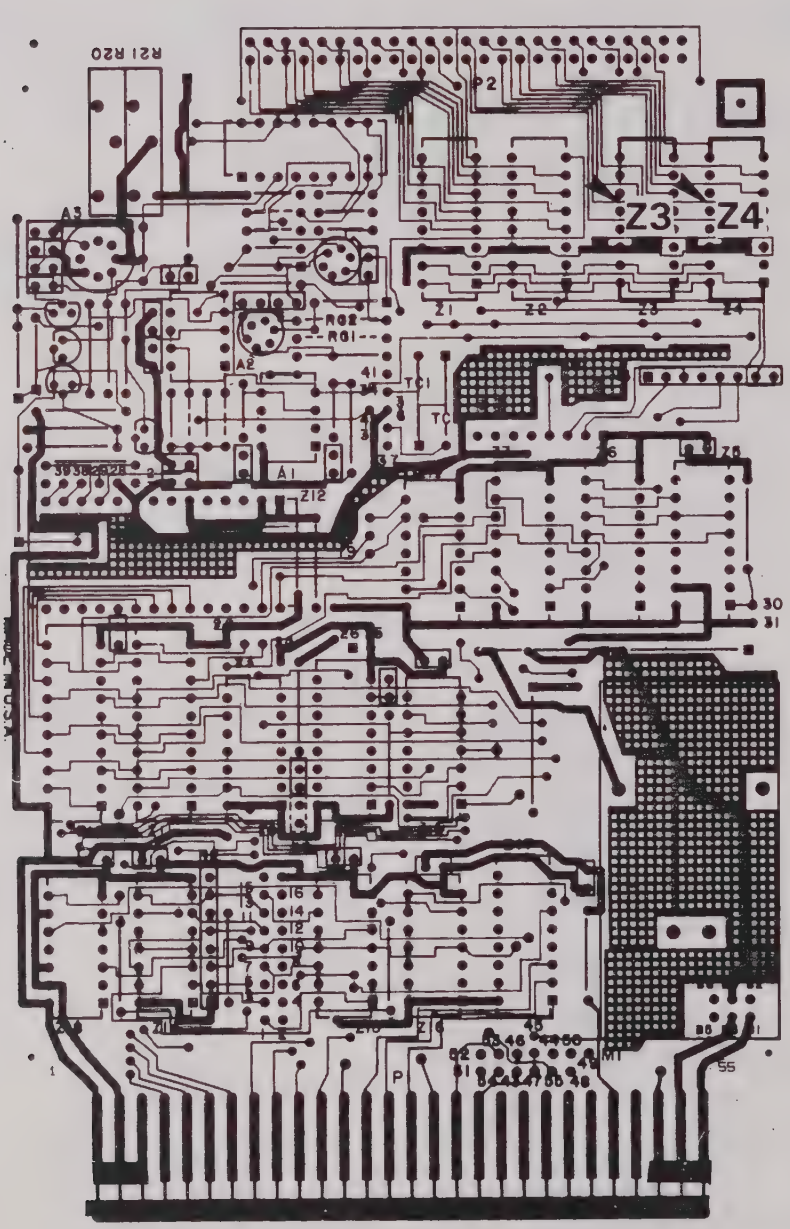
Note: Pins 50 and 52 are same node.

LOCAL SENSE

D/A	Jumper
DAC0	28 to 29
DAC1	30 to 31
DAC2	32 to 33
DAC3	34 to 35

APPENDIX G

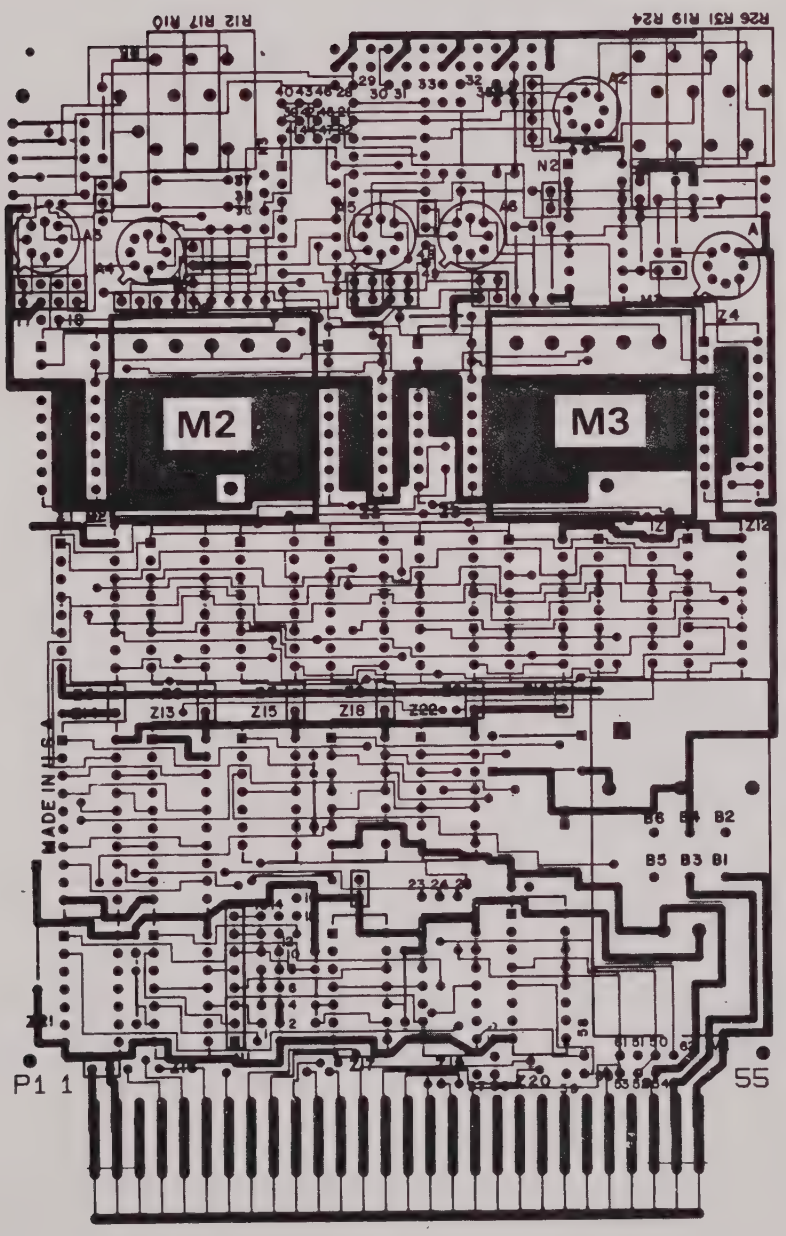
WIRE WRAP AND ACCESSORY LOCATIONS



RTI-1260

APPENDIX G

WIRE WRAP AND ACCESSORY LOCATIONS



RTI-1262

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ERRATA SHEET

7806/7807 Z80A Multifunction CPU Cards USER'S MANUAL

BIPOLAR PROM REPLACEMENT

The Harris 7648-5 bipolar PROM is currently out of production. Pro-Log has qualified an AMD bipolar PROM to take its place. To reflect this change, please replace Figure 2-7 on page 2-10 of the 7806/7807 User's Manual (Pro-Log document #110139-002D) with the following table:

	PRO-LOG PROM PROGRAMMING EQUIPMENT*		
PROM Part Number	Personality Module	Pinout Adapter	Configurator
MMI 6348-1	PM9037	PA20-1	512x8 (H)
AMD AM27S28	PM9058	PA20-4	512x8 (L)

*The equipment listed must be used in conjunction with any Pro-Log Series 90 PROM Programmer.

Figure 2-7. Decoder PROM Part Numbers and Programming Equipment (7806/7807)

Timing Figures

Correct the timing figures as follows:

	4 MHz	2.5 MHz
Page 2-15, Figure 2-11:		
tS4 Data setup before RD* inactive	85 MIN.	100 MIN.
Page 2-16, Figure 2-12:		
tS4 Data setup before RD* inactive	175 TYP.	210 TYP.
Page 2-17, Figure 2-15:		
tS4 Data setup before RD* inactive	175 TYP.	210 TYP.

In **Figure 3-5** on page 3-12, the figures listed under CTC COUNT for the 2.5 MHz version are reversed. The figures listed under the decimal (DEC) subheading should be under the hexadecimal (HEX) subheading and vice versa.

PROGRAMMED MEMORY MAPPING OPTIONS

The number of preprogrammed options in the memory decoder PROM has been increased from 7 to 14. This change needs to be made on the first and second paragraphs of page 2-6 and the second paragraph of page 2-8. Replace the table of Figure 2-5 (page 2-7) with the following table:

OPTION #	A8[1]	A7[2]	A6	A5	SOCKET 0	SOCKET 1	SOCKET 2	SOCKET 3
0	LO	LO	LO	LO	4K 0000-0FFF	4K 1000-1FFF	4K 2000-2FFF	2K 3000-3FFF
1	LO	LO	LO	HI	8K 0000-1FFF	8K 2000-3FFF	8K 4000-5FFF	8K 6000-7FFF
2	LO	LO	HI	LO	16K 0000-3FFF	16K 4000-7FFF	8K 8000-9FFF	8K A000-BFFF
3	LO	LO	HI	HI	32K 0000-7FFF	8K 8000-9FFF	8K A000-BFFF	8K C000-DFFF
4	LO	HI	LO	LO	4K 0000-0FFF	4K 1000-1FFF	4K 2000-2FFF	4K 3000-3FFF
5	LO	HI	LO	HI	16K 0000-3FFF	12K[3] 4000-6FFF	2K 7000-77FF	2K 7800-7FFF
6	LO	HI	HI	LO	2K 0000-07FF	2K 0800-0FFF	2K 1000-17FF	2K 1800-1FFF
7	LO	HI	HI	HI	UNPROGRAMMED. MAY BE PROGRAMMED BY THE USER			
8	HI	LO	LO	LO	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED
9	HI	LO	LO	HI	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED
10	HI	LO	HI	LO	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED
11	HI	LO	HI	HI	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED
12	HI	HI	LO	LO	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED
13	HI	HI	LO	HI	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED
14	HI	HI	HI	LO	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED	SOCKET DISABLED
15	LO	HI	HI	HI	UNPROGRAMMED. MAY BE PROGRAMMED BY THE USER			

NOTE: With jumper W12 configured as shipped and with MEMEX low, as it is after power-up or reset, option #0 is selected
[1]May be connected to MEMEX
[2]May be connected to SEGMENT
[3]Requires a 16K device installed, but only 12K of the device may be accessed.

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